E614 DAQ

Specifications
Hardware
Software

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E614 DAQ
Specifications

- Multi-hit TDC capability
- Trigger Rate : 5000 events/s
- Event size : 1000 B/event
- Lowest possible deadtime

This usually means we have to be ready to handle twice the trigger rate and twice the data size.

Conclusion

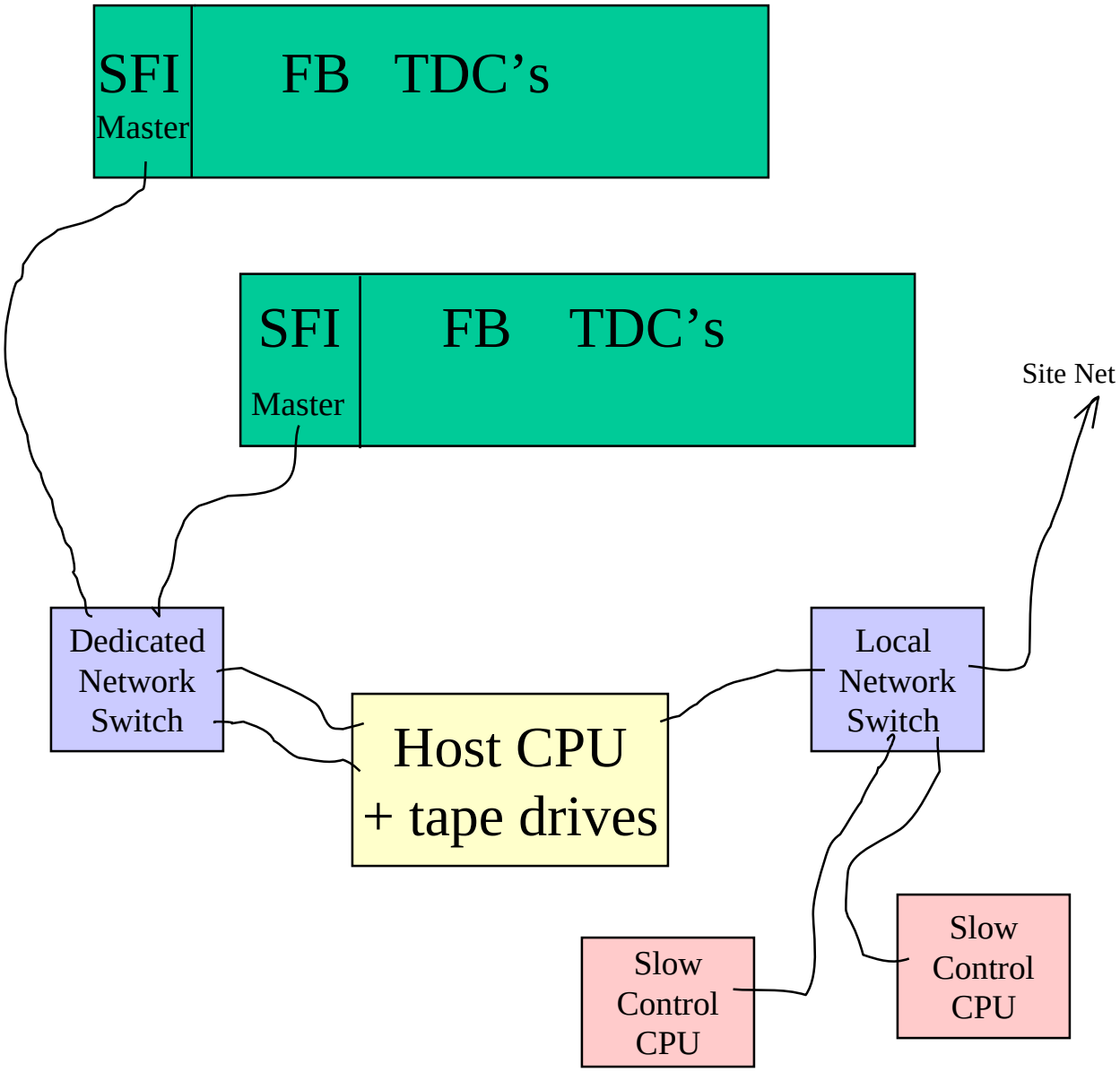
Design a system for 10 - 20 MB/s throughput

E614 DAQ

- Channel Count for 1/2 of the detector

	Wires/plane		# of planes	TDC channels	ADC channels
	Total	Instru-mented			
Central PC's	160	32	2	64	64
PDC pairs	80	80	16	1280	-
Dense PDC	80	48	6	288	-
Outer PC's	160	32 (2x)64	4	128 256	-
Total for Chambers				2016 (21x96)	64
Scint				2	2
Muon Chambers				32 one side	

E614 DAQ overview



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E614 DAQ
Hardware

- Fastbus System
  - 2 or 3 FB crates
  - FB Master = SFI (Struck Fastbus Interface)
    - Fastbus sequencer with list processor
    - Block transfer handshake: DS = 35 ns
    - VME backplane for commercial VME CPU
  - Struck Company has folded but two companies are now in competition to offer the SFI.
  - CEBAF has ~ 40 SFI's and BNL E787 has 6 SFI

- Front end processor
  - PPC 604 @ 300 MHz : MVME 2306
  - Fast Ethernet connection (100 BaseT) to network switch
  - VxWorks realtime operating system

E614 DAQ
Hardware

- TDC's : Lecroy 1877 Multihit pipelined TDC
  - Specs:
    - 96 Channels Per FASTBUS Slot
    - 500 psec LSB
    - Programmable Full Scale up to 32 µsec
    - Up to 16 Edges/Channel (Programmable)
    - Rising and/or Falling Edge Timing Information
    - < 20 nsec Double Pulse Resolution
    - Built-in Data Zero Suppression and Data Compaction
  - There are two versions of this TDC
  - The 1877 :
    - Input signals converted to TTL and bussed to the auxiliary connector are available for trigger processor.
    - Fast Conversion: 1.2 µsec + 50 nsec per hit; 1.75 µsec minimum.
    - Price quoted to BNL in March 1998 : US$ 7700. (~$80./ch)..
  - The 1877S:
    - No input signals bussed to the aux. connector
    - A minimum width to convert signal can be downloaded on an individual channel basis. This allows rejection of narrow signals or use of the device as an ADC when used with a front end charge-to-time converter chip (for example the MQT300a)
    - Fast Conversion: 1.2 µsec + 50 nsec per hit; 1.75 µsec minimum.
    - Price quoted to BNL in March 1998 : US$ 7000 thus 10% cheaper than 1877 (~$73./ch)

E614 DAQ
Hardware

- ADC’s -Two options :

  - FB 1881M ADC : 64 ch /board
    - High Density, 64 Channels Per FASTBUS Slot
    - Short Conversion Time, 12 µsec in 13-Bit Mode (9 µsec in 12-Bit Mode)
    - Full 13-Bit Resolution Above Pedestal
    - High Sensitivity, 50 fC/count
    - Sparse Data Readout
    - Price quoted to BNL in March 1998 : US$ 6640. (~$105./ch)

  - MQT300a chip + 1877s TDC's
    - Wide Dynamic Range: 18-Bit with 12-Bit Precision
    - Short Rundown Time: < 6 µsec (for ranges in linear region)
    - Programmable Sensitivity: 10 fC/ns to 640 fC/ns in 3 Ranges
    - 28-Pin PLCC Package
    - 2620 pC Full Scale Range Beyond Pedestal
    - Differential ECL Outputs and Gate Input for Enhanced Noise Immunity
    - High Noise Immunity

E614 DAQ
Timings

- Two FB crates should be sufficient to house
  - 3 slots : SFI master + PPC
  - 21 slots : TDC's for chambers
  - 1 slot : TDC for ADC & muon chambers
  - 1 spare slot or IO board with 20ns clock counter for synchronization
- Trigger deadtime：
  - 10 micros/ev @ 5K ev/s = 50 ms = 5 %
- Readout deadtime:
  - It is equal to readout time of TDC with maximum number of hits because of the event buffering capabilities of the TDC.

    Maximum is 14 micros/ev @ 5K ev/s = 70 ms = 7 %
- SFI Readout time:
  - Does not contribute to deadtime as long as the readout can proceed without bottlenecks
  - Events are read out as one 32 bit block transfer at the rate of < 150 ns/transfer

  1KB = 250 words/ev @5000 ev/s @ 150 ns = 187 ms

E614 DAQ
Timings

- Data transfer time to host:
  - Uses two 100BaseT Ethernet channels into a network switch connected to the host CPU via two other Ethernet ports. This gives two parallel streams capable of running at > 9 MB/s each for an aggregate throughput of 18 MB/s. If 2 streams are not sufficient we could add a 3rd FB crate for a 3rd stream.
- Data logging:
  - Use parallel DLT7000 tape drives, each running at 5 MB/s capable of storing > 40 GB
- Host system:
  - Experience with an SGI Origin 200 (4 CPU) shows that the input transfer rates, data logging and data monitoring are possible NOW. By the time we have to purchase the host, there should be even more powerful system available.
- Funding for the FB crates, SFI + PPC, host CPU and DLT drives comes from the TRIUMF DAQ budget with components available next fall.
- Funding for the TDC's comes from DOE. Ordering of the TDC's must be done soon to get delivery by fall 1999.

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E614 DAQ
Software

- MIDAS
  - Acquires data and makes events available to other processes
  - Provides logging to disk and/or tape
  - Slow control support
  - Web based user interface
  - Libraries exist for several platforms
    - UNIX: Ultrix, Linux, Digital Unix
    - VxWorks
    - Windows NT, Windows ‘95, DOS
    - VMS

- Online monitoring
  - Will be done with analysis software
  - HBOOK and PAW
  - Event display using ROOT

E614 DAQ
Beam test system

- Beam tests in August 1997 were done with a FB system using :
  - SFI master + VME 68040 processor
  - 2 TDC 1877
  - Camac SADC for pressure and temperature measurement
  - Ultrix Decstation plus Exabyte drive for logging and user control
  - Alpha Digital Unix Decstation for monitoring software and event display
  - MIDAS software

E614 DAQ
1999 development schedule

- Feb - April :
  - Install Power PC in SFI
  - Test mixed 1877 and 1877s
  - Test the full prototype XY DC pair
- June - Oct :
  - Develop code using multievent buffers in the TDC's
  - develop test procedures for full electronic chain
- Nov - Dec :
  - Test a full crate (need 20 new TDC's)
  - Add slow control computer to system